

1     WHAT IS CLAIMED IS

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1. A semiconductor device, comprising:

a mount substrate;

a high-frequency transmission line provided on  
a top surface of said mount substrate;

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a semiconductor chip mounted on said top  
surface of said mount substrate in a facedown state in  
electrical contact with said high-frequency transmission  
line, said semiconductor chip thereby having a bottom  
surface facing said top surface of said mount substrate;

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and

a depression formed on said top surface of  
said mount substrate.

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2. A semiconductor device as claimed in claim  
1, wherein said semiconductor chip carries a projection  
on said bottom surface, said semiconductor chip being  
25 mounted on said top surface of said mount substrate such

1     that said projection is accepted into said depression,  
and wherein said depression has a depth set such that  
said projection does not contact a surface of said  
depression.

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3. A semiconductor device as claimed in claim  
10    2, further comprising an interconnection structure on  
said high-frequency transmission line, said  
semiconductor chip being connected electrically and  
mechanically to said high-frequency transmission line  
via said interconnection structure, wherein said depth  
15    of said depression is set such that said depth is equal  
to or larger than a height of said projection from which  
a height of said interconnection structure is  
subtracted.

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4. A semiconductor device as claimed in claim  
3, wherein said interconnection structure includes a  
25    solder bump.

1           5. A semiconductor device as claimed in claim  
2, wherein said semiconductor chip carries a coplanar  
transmission line on said bottom surface thereof, and  
wherein said projection is an air bridge structure  
5 forming a part of said coplanar transmission line.

10           6. A semiconductor device as claimed in claim  
1, wherein said depression forms a through-hole  
penetrating through said mount substrate from said top  
surface to a bottom surface opposite to said top  
surface.

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          7. A semiconductor device as claimed in claim  
20 1, wherein said high-frequency transmission line is a  
microstrip line including a ground layer, a dielectric  
layer provided on said ground layer and a wiring layer  
provided on said dielectric layer.

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1           8. A semiconductor device as claimed in claim  
7, wherein said dielectric layer is formed of  $\text{SiO}_2$ .

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          9. A semiconductor device as claimed in claim  
7, wherein said dielectric layer is formed of polyimide.

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          10. A semiconductor device as claimed in  
claim 1, wherein said substrate is formed of Si.

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          11. A semiconductor device as claimed in  
20 claim 1, wherein said substrate is formed of polyimide.

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          12. A semiconductor device as claimed in

1 claim 1, wherein said depression is defined by a crystal  
surface.

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13. A method of fabricating a semiconductor  
device comprising a mount substrate; a high-frequency  
transmission line provided on a top surface of said  
10 mount substrate; a semiconductor chip mounted on said  
top surface of said mount substrate in a facedown state  
in electrical contact with said high-frequency  
transmission line, said semiconductor chip thereby  
having a bottom surface facing said top surface of said  
15 mount substrate; and a depression formed on said top  
surface of said mount substrate, said semiconductor chip  
carrying an air bridge structure on said bottom surface,  
said method comprising a steps of:

forming said depression by an etching process  
20 to said top surface of said mount substrate; and  
mounting said semiconductor chip on said mount  
substrate such that said air bridge structure is  
accommodated into said depression.

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1           14. A method as claimed in claim 13, wherein  
said mount substrate is formed of Si, and wherein said  
etching step includes an anisotropic wet etching process  
applied to said top surface of said mount substrate.

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          15. A method as claimed in claim 13, wherein  
10 said mount substrate is formed of polyimide, and wherein  
said etching step includes a dry etching process applied  
to said top surface of said mount substrate.

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